WHAT IS CLAIMED IS:

1. A microcomputer, comprising:

a CPU;

a plurality of signal lines provided corresponding to an output signal of said CPU;

a data memory part being capable of storing a setting data corresponding to said plurality of signal lines on the basis of an external signal;

a first signal transmitting means transmitting said output signal of said CPU to said plurality of signal lines in an active state;

a second signal transmitting means transmitting said setting data of said data memory part to said plurality of signal lines in an active state; and

signal transmitting control means controlling an activity / an inactivity of said first and second signal transmitting means; wherein

said signal transmitting control means receives a mode signal, and forces only said first signal transmitting means to be in an active state when said mode signal indicates a normal state, and forces only said second signal transmitting means to be in an active state when said mode signal indicates a special state.

2. The microcomputer according to claim 1, wherein

said external signal includes a serial data, and

said data memory part includes a data memory part having multibit structure and storing said setting data by taking in said external signal with shifting.

3. The microcomputer according to claim 2, wherein

said data memory part includes a data memory part employed as a serial I/O in a normal action of said microcomputer.

4. The microcomputer according to claim 1, wherein

said external signal includes a timing signal performing a predetermined signal transition change at a predetermined timing, and

said data memory part includes a data memory part having multibit structure and counting a number of said predetermined signal transition change of said timing signal as said setting data.

5. The microcomputer according to claim 4, wherein

said data memory part includes a data memory part employed as a timer in a normal action of said microcomputer.

6. A microcomputer, comprising:

a CPU outputting a multibit address signal for selection of a word line;

a memory part having a plurality of word lines;

a main decoder performing a decode processing on the basis of a main address signal except for a least significant bit address signal in said address signal to obtain a main decode result;

a sub-decode part receiving said main decode result, said least significant bit address signal and a mode signal, and performing a potential setting of said plurality of word lines; wherein

when said mode signal indicates a normal state, said sub-decode part sets one of said plurality of word lines to a potential in a selective state on the basis of said main

decode result and said least significant bit address signal, and when said mode signal indicates a special state, said sub-decode part performs a potential setting of said plurality of word lines only on the basis of said least significant bit address signal.

7. A microcomputer, comprising:

a CPU outputting a multibit address signal;

a memory part having a plurality of word lines and a plurality of bit lines;

a word line selecting means receiving a mode signal, selecting one of plurality of word lines on the basis of said address signal when said mode signal indicates a normal state, and forcing all of said plurality of word lines to be in non-selective state when said mode signal indicates a special state; and

a bit line potential setting part receiving said mode signal, being in an active state when said mode signal indicates a special state and performing a potential setting of said plurality of bit lines in a predetermined mode.